Mohamed H. Abu-Rahma · Mohab Anis

Nanometer Variation-Tolerant SRAM

Circuits and Statistical Design for Yield

Springer

Nanometer Variation Tolerant Sram Circuits And Statistical Design For Yield

Victor Champac,Jose Garcia Gervacio

Nanometer Variation Tolerant Sram Circuits And Statistical Design For Yield:

Nanometer Variation-Tolerant SRAM Mohamed Abu Rahma,Mohab Anis,2012-09-26 Variability is one of the most challenging obstacles for IC design in the nanometer regime In nanometer technologies SRAM show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density With the drastic increase in memory densities lower supply voltages and higher variations statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies Provides comprehensive review of state of the art variation tolerant SRAM circuit techniques Discusses Impact of device related process variations and how they affect circuit and system performance from a design point of view Helps designers optimize memory yield with practical statistical design methodologies and yield estimation techniques Low-Power Variation-Tolerant Design in Nanometer Silicon Swarup Bhunia,Saibal Mukhopadhyay,2010-11-10 Design considerations for low power operations and robustness with respect to variations typically impose contradictory requirements Low power design techniques such as voltage scaling dual threshold assignment and gate sizing can have large negative impact on parametric yield under process variations This book focuses on circuit architectural design techniques for achieving low power operation under parameter variations We consider both logic and memory design aspects and cover modeling and analysis as well as design methodology to achieve simultaneously low power and variation tolerance while minimizing design overhead This book will discuss current industrial practices and emerging challenges at future technology nodes

Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS Nodes Hsiao-Hsuan Liu,Francky Catthoor,2024-12-20 Modern computing engines CPUs GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline

effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes *Data Science and Applications* Satyasai Jagannath Nanda,Rajendra Prasad Yadav,Amir H. Gandomi,Mukesh Saraswat,2024-02-24 This book gathers outstanding papers presented at the International Conference on Data Science and Applications ICDSA 2023 organized by Soft Computing Research Society SCRS and Malaviya National Institute of Technology Jaipur India from 14 to 15 July 2023 The book is divided into four volumes and it covers theoretical and empirical developments in various areas of big data analytics big data technologies decision tree learning wireless communication wireless sensor networking bioinformatics and systems artificial neural networks deep learning genetic algorithms data mining fuzzy logic optimization algorithms image processing computational intelligence in civil engineering and creative computing **Microelectronics, Electromagnetics and Telecommunications** Jaume Anguera,Suresh Chandra Satapathy,Vikrant Bhateja,K.V.N. Sunitha,2018-01-25 The volume contains 94 best selected research papers presented at the Third International Conference on Micro Electronics Electromagnetics and Telecommunications ICMEET 2017 The conference was held during 09 10 September 2017 at Department of Electronics and Communication Engineering BVRIT Hyderabad College of Engineering for Women Hyderabad Telangana India The volume includes original and application based research papers on microelectronics electromagnetics telecommunications wireless communications signal speech video processing and embedded systems **Timing Performance of Nanometer Digital Circuits Under Process Variations** Victor Champac,Jose Garcia Gervacio,2018-04-18 This book discusses the digital design of integrated circuits under process variations with a focus on design time solutions The authors describe a step by step methodology going from logic gates to logic paths to the circuit level Topics are presented in comprehensively without overwhelming use of analytical formulations Emphasis is placed on providing digital designers with understanding of the sources of process variations their impact on circuit performance and tools for improving their designs to comply with product specifications Various circuit level design hints are highlighted so that readers can use then to improve their designs A special treatment is devoted to unique design issues and the impact of

process variations on the performance of FinFET based circuits This book enables readers to make optimal decisions at design time toward more efficient circuits with better yield and higher reliability **Computing with Memory for Energy-Efficient Robust Systems** Somnath Paul,Swarup Bhunia,2013-09-07 This book analyzes energy and reliability as major challenges faced by designers of computing frameworks in the nanometer technology regime The authors describe the existing solutions to address these challenges and then reveal a new reconfigurable computing platform which leverages high density nanoscale memory for both data storage and computation to maximize the energy efficiency and reliability The energy and reliability benefits of this new paradigm are illustrated and the design challenges are discussed Various hardware and software aspects of this exciting computing paradigm are described particularly with respect to hardware software co designed frameworks where the hardware unit can be reconfigured to mimic diverse application behavior Finally the energy efficiency of the paradigm described is compared with other well known reconfigurable computing platforms **AI-Enabled Electronic Circuit and System Design** Ali Iranmanesh,Hossein Sayadi,2025-01-27 As our world becomes increasingly digital electronics underpin nearly every industry Understanding how AI enhances this foundational technology can unlock innovations from smarter homes to more powerful gadgets offering vast opportunities for businesses and consumers alike This book demystifies how AI streamlines the creation of electronic systems making them smarter and more efficient With AI s transformative impact on various engineering fields this resource provides an up to date exploration of these advancements authored by experts actively engaged in this dynamic field Stay ahead in the rapidly evolving landscape of AI in engineering with AI Enabled Electronic Circuit and System Design From Ideation to Utilization your essential guide to the future of electronic systems endif A transformative guide describing how revolutionizes electronic design through AI integration Highlighting trends challenges and opportunities Demystifies complex AI applications in electronic design for practical use Leading insights authored by top experts actively engaged in the field Offers a current relevant exploration of significant topics in AI s role in electronic circuit and system design Editor s bios Dr Ali A Iranmanesh is the founder and CEO of Silicon Valley Polytechnic Institute He has received his Bachelor of Science in Electrical Engineering from Sharif University of Technology SUT Tehran Iran and both his master s and Ph D degrees in Electrical Engineering and Physics from Stanford University in Stanford CA He additionally holds a master s degree in business administration MBA from San Jose State University in San Jose CA Dr Iranmanesh is the founder and chairman of the International Society for Quality Electronic Design ISQED Currently he serves as the CEO of Innovotek Dr Iranmanesh has been instrumental in advancing semiconductor technologies innovative design methodologies and engineering education He holds nearly 100 US and international patents reflecting his signifi cant contributions to the field Dr Iranmanesh is the Senior life members of EEE senior member of the American Society for Quality co founder and Chair Emeritus of the IEEE Education Society of Silicon Valley Vice Chair Emeritus of the IEEE PV chapter and recipient of IEEE Outstanding Educator Award Dr Hossein Sayadi is a

Tenure Track Assistant Professor and Associate Chair in the Department of Computer Engineering and Computer Science at California State University Long Beach CSULB He earned his Ph D in Electrical and Computer Engineering from George Mason University in Fairfax Virginia and an M Sc in Computer Engineering from Sharif University of Technology in Tehran Iran As a recognized researcher with over 14 years of research experience Dr Sayadi is the founder and director of the Intelligent Secure and Energy Efficient Computing iSEC Lab at CSULB His research focuses on advancing hardware security and trust AI and machine learning cybersecurity and energy efficient computing addressing critical challenges in modern computing and cyber physical systems He has authored over 75 peer reviewed publications in leading conferences and journals Dr Sayadi is the CSU STEM NET Faculty Fellow with his research supported by multiple National Science Foundation NSF grants and awards from CSULB and the CSU Chancellor s Office He has contributed to various international conferences as an organizer and program committee member including as the TPC Chair for the 2024 and 2025 IEEE ISQED

Design of Variation-tolerant Circuits for Nanometer CMOS Technology Mohamed Hassan Abu-Rahma,2008 Aggressive scaling of CMOS technology in sub 90nm nodes has created huge challenges Variations due to fundamental physical limits such as random dopants fluctuation RDF and line edge roughness LER are increasing significantly with technology scaling In addition manufacturing tolerances in process technology are not scaling at the same pace as transistor s channel length due to process control limitations e g sub wavelength lithography Therefore within die process variations worsen with successive technology generations These variations have a strong impact on the maximum clock frequency and leakage power for any digital circuit and can also result in functional yield losses in variation sensitive digital circuits such as SRAM Moreover in nanometer technologies digital circuits show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density It is therefore not surprising that the International Technology Roadmap for Semiconductors ITRS lists variability as one of the most challenging obstacles for IC design in nanometer regime To facilitate variation tolerant design we study the impact of random variations on the delay variability of a logic gate and derive simple and scalable statistical models to evaluate delay variations in the presence of within die variations This work provides new design insight and highlights the importance of accounting for the effect of input slew on delay variations especially at lower supply voltages **Nanometer Variation-Tolerant Sram** ,2012-09-28 *Statistical Yield Analysis and Design for Nanometer VLSI* Javid Jaffari,2010 Process variability is the pivotal factor impacting the design of high yield integrated circuits and systems in deep sub micron CMOS technologies The electrical and physical properties of transistors and interconnects the building blocks of integrated circuits are prone to significant variations that directly impact the performance and power consumption of the fabricated devices severely impacting the manufacturing yield However the large number of the transistors on a single chip adds even more challenges for the analysis of the variation effects a critical task in diagnosing the

cause of failure and designing for yield Reliable and efficient statistical analysis methodologies in various design phases are key to predict the yield before entering such an expensive fabrication process In this thesis the impacts of process variations are examined at three different levels device circuit and micro architecture The variation models are provided for each level of abstraction and new methodologies are proposed for efficient statistical analysis and design under variation Robust Design of Variation-sensitive Digital Circuits Hassan Mostafa,2011 The nano age has already begun where typical feature dimensions are smaller than 100nm The operating frequency is expected to increase up to 12 GHz and a single chip will contain over 12 billion transistors in 2020 as given by the International Technology Roadmap for Semiconductors ITRS initiative ITRS also predicts that the scaling of CMOS devices and process technology as it is known today will become much more difficult as the industry advances towards the 16nm technology node and further This aggressive scaling of CMOS technology has pushed the devices to their physical limits Design goals are governed by several factors other than power performance and area such as process variations radiation induced soft errors and aging degradation mechanisms These new design challenges have a strong impact on the parametric yield of nanometer digital circuits and also result in functional yield losses in variation sensitive digital circuits such as Static Random Access Memory SRAM and flip flops Moreover sub threshold SRAM and flip flops circuits which are aggravated by the strong demand for lower power consumption show larger sensitivity to these challenges which reduces their robustness and yield Accordingly it is not surprising that the ITRS considers variability and reliability as the most challenging obstacles for nanometer digital circuits robust design Soft errors are considered one of the main reliability and robustness concerns in SRAM arrays in sub 100nm technologies due to low operating voltage small node capacitance and high packing density The SRAM arrays soft errors immunity is also affected by process variations We develop statistical design oriented soft errors immunity variations models for super threshold and sub threshold SRAM cells accounting for die to die variations and within die variations This work provides new design insights and highlights the important design knobs that can be used to reduce the SRAM cells soft errors immunity variations The developed models are scalable bias dependent and only require the knowledge of easily measurable parameters This makes them useful in early design exploration circuit optimization as well as technology prediction The derived models are verified using Monte Carlo SPICE simulations referring to an industrial hardware calibrated 65nm CMOS technology The demand for higher performance leads to very deep pipelining which means that hundreds of thousands of flip flops are required to control the data flow under strict timing constraints A violation of the timing constraints at a flip flop can result in latching incorrect data causing the overall system to malfunction In addition the flip flops power dissipation represents a considerable fraction of the total power dissipation Sub threshold flip flops are considered the most energy efficient solution for low power applications in which performance is of secondary importance Accordingly statistical gate sizing is conducted to different flip flops topologies for timing yield improvement of super threshold flip flops and power yield improvement of sub threshold flip

flops Following that a comparative analysis between these flip flops topologies considering the required overhead for yield improvement is performed This comparative analysis provides useful recommendations that help flip flops designers on selecting the best flip flops topology that satisfies their system specifications while taking the process variations impact and robustness requirements into account Adaptive Body Bias ABB allows the tuning of the transistor threshold voltage Vt by controlling the transistor body voltage A forward body bias reduces Vt increasing the device speed at the expense of increased leakage power Alternatively a reverse body bias increases Vt reducing the leakage power but slowing the device Therefore the impact of process variations is mitigated by speeding up slow and less leaky devices or slowing down devices that are fast and highly leaky Practically the implementation of the ABB is desirable to bias each device in a design independently to mitigate within die variations However supplying so many separate voltages inside a die results in a large area overhead On the other hand using the same body bias for all devices on the same die limits its capability to compensate for within die variations Thus the granularity level of the ABB scheme is a trade off between the within die variations compensation capability and the associated area overhead This work introduces new ABB circuits that exhibit lower area overhead by a factor of 143X than that of previous ABB circuits In addition these ABB circuits are resolution free since no digital to analog converters or analog to digital converters are required on their implementations These ABB circuits are adopted to high performance critical paths emulating a real microprocessor architecture for process variations compensation and also adopted to SRAM arrays for Negative Bias Temperature Instability NBTI aging and process variations compensation The effectiveness of the new ABB circuits is verified by post layout simulation results and test chip measurements using triple well 65nm CMOS technology The highly capacitive nodes of wide fan in dynamic circuits and SRAM bitlines limit the performance of these circuits In addition process variations mitigation by statistical gate sizing increases this capacitance further and fails in achieving the target yield improvement We propose new negative capacitance circuits that reduce the overall parasitic capacitance of these highly capacitive nodes These negative capacitance circuits are adopted to wide fan in dynamic circuits for timing yield improvement up to 99 87% and to SRAM arrays for read access yield improvement up to 100% The area and power overheads of these new negative capacitance circuits are amortized over the large die area of the microprocessor and the SRAM array The effectiveness of the new negative capacitance circuits is verified by post layout simulation results and test chip measurements using 65nm CMOS technology **Robust Optimization of Nanometer SRAM Designs** Akshit Dayal,2011 Technology scaling has been the most obvious choice of designers and chip manufacturing companies to improve the performance of analog and digital circuits With the ever shrinking technological node process variations can no longer be ignored and play a significant role in determining the performance of nanoscaled devices By choosing a worst case design methodology circuit designers have been very munificent with the design parameters chosen often manifesting in pessimistic designs with significant area overheads Significant work has been done

in estimating the impact of intra die process variations on circuit performance pertinently noise margin and standby leakage power for fixed transistor channel dimensions However for an optimal high yield SRAM cell design it is absolutely imperative to analyze the impact of process variations at every design point especially since the distribution of process variations is a statistically varying parameter and has an inverse correlation with the area of the MOS transistor Furthermore the first order analytical models used for optimization of SRAM memories are not as accurate and the impact of voltage and its inclusion as an input along with other design parameters is often ignored In this thesis the performance parameters of a nano scaled 6 T SRAM cell are modeled as an accurate yield aware empirical polynomial predictor in the presence of intra die process variations The estimated empirical models are used in a constrained non linear robust optimization framework to design an SRAM cell for a 45 nm CMOS technology having optimal performance according to bounds specified for the circuit performance parameters with the objective of minimizing on chip area This statistically aware technique provides a more realistic design methodology to study the trade off between performance parameters of the SRAM Furthermore a dual optimization approach is followed by considering SRAM power supply and wordline voltages as additional input parameters to simultaneously tune the design parameters ensuring a high yield and considerable area reduction In addition the cell level optimization framework is extended to the system level optimization of caches under both cell level and system level performance constraints *Overcoming the Circuit Design Challenges in Nanoscale SRAMs* ,2006 Most microprocessors use large on chip SRAM caches to bridge the performance gap between the processor and the main memory Due to their growing embedded applications coupled with the technology scaling challenges considerable attention is given to the design of low power and high performance SRAMs However there are many challenges in the design of both embedded and stand alone SRAMs such as the estimation and optimization of stand by power design of high speed peripheral circuits and design of robust circuits for low voltage operation Further as the technology continues scaling into the nanometer domain controlling the variation in device parameters during fabrication becomes a great challenge Variations in process parameters such as oxide thickness channel length channel width and dopant concentration can result in large variations in threshold voltage This in turn is expected to severely affect the functionality of the minimum geometry transistors that are commonly used in SRAM designs Our studies of new memory and peripheral circuits have shown significant promise in terms of power speed and robustness In this research we address the following problems 1 Circuit techniques to estimate and simultaneously reduce gate leakage and sub threshold leakage 2 Process variations tolerant design approaches to reliably sense and amplify the bitlines with a minimum discharge providing a fast and accurate readout at low power 3 Failure analysis to understand the impact of process variations soft errors leakage and noise on different memory fault mechanism to help in the design of variation tolerant low power and high performance memories 4 Design of test structures for CMOS process tuning and variation control and improvement of SRAM reliability by predicting the design yield early in the product

cycle In short this dissertation characterizes the issues in nanoscale memory design which will have a ubiquitous presence in commercial electronic market It is important for these systems to be reliable fast and consume less power thereby increasing battery life Design techniques to achieve these goals are presented **Robust SRAM Designs and Analysis** Jawar Singh,Saraju P. Mohanty,Dhiraj K. Pradhan,2012-08-01 This book provides a guide to Static Random Access Memory SRAM bitcell design and analysis to meet the nano regime challenges for CMOS devices and emerging devices such as Tunnel FETs Since process variability is an ongoing challenge in large memory arrays this book highlights the most popular SRAM bitcell topologies benchmark circuits that mitigate variability along with exhaustive analysis Experimental simulation setups are also included which cover nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Emphasis is placed throughout the book on the various trade offs for achieving a best SRAM bitcell design Provides a complete and concise introduction to SRAM bitcell design and analysis Offers techniques to face nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Includes simulation set ups for extracting different design metrics for CMOS technology and emerging devices Emphasizes different trade offs for achieving the best possible SRAM bitcell design *Nanometer SRAM and DRAM Circuit Design* Paul S. Lazar,Yong-Bin Kim,Ban P. Wong,2015-03-02 Low power consumption is moving higher up on the priority list of system requirements resulting in low power memory architectures and circuit implementations Circuits need to operate reliably at low voltages below 1 0V yet meet their performance targets The larger spread of process variations as the technology node shrinks makes worst case design impractical These design challenges impact also the peripheral control ancillary and i o circuits of the SRAM and DRAM The goal of this book is to describe circuits and circuit design methodologies which overcome these challenges Examples of scripts which are used to steer the CAD tools used in the analysis of the circuits and to gather and present the results of such analysis are provided Since a variety of the emerging technologies such as CNT Carbon Nano Tube and FinFET are being developed and researched a new design method for memory cell will also be discussed based on those emerging technologies

Robust SRAM Designs and Analysis Jawar Singh,Saraju P. Mohanty,Dhiraj Pradhan,2014-08-08 This book provides a guide to Static Random Access Memory SRAM bitcell design and analysis to meet the nano regime challenges for CMOS devices and emerging devices such as Tunnel FETs Since process variability is an ongoing challenge in large memory arrays this book highlights the most popular SRAM bitcell topologies benchmark circuits that mitigate variability along with exhaustive analysis Experimental simulation setups are also included which cover nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Emphasis is placed throughout the book on the various trade offs for achieving a best SRAM bitcell design Provides a complete and concise introduction to SRAM bitcell design and analysis Offers techniques to face nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Includes simulation set ups for extracting different design metrics for CMOS technology and emerging devices Emphasizes

different trade offs for achieving the best possible SRAM bitcell design *Statistical Methodologies for Modelling the Impact of Process Variability in Ultra-deep-submicron SRAMs* Kaya Can Akyel,2014 The downscaling of device geometry towards its physical limits exacerbates the impact of the inevitable atomistic phenomena tied to matter granularity In this context many different variability sources raise and affect the electrical characteristics of the manufactured devices The variability aware design methodology has therefore become a popular research topic in the field of digital circuit design since the increased number of transistors in the modern integrated circuits had led to a large statistical variability affecting dramatically circuit functionality Static Random Access Memory SRAM circuits which are manufactured with the most aggressive design rules in a given technology node and contain billions of transistor are severely impacted by the process variability which stands as the main obstacle for the further reduction of the bitcell area and of its minimum operating voltage The reduction of the latter is a very important parameter for Low Power design which is one of the most popular research fields of our era The optimization of SRAM bitcell design therefore has become a crucial task to guarantee the good functionality of the design at an industrial manufacturing level in the same time answering to the high density and low power demands However the long time required by each new technology node process development means a long waiting time before obtaining silicon results which is in cruel contrast with the fact that the design optimization has to be started as early as possible An efficient SPICE characterization methodology for the minimum operating voltage of SRAM circuits is therefore a mandatory requirement for design optimization This research work concentrates on the development of the new simulation methodologies for the modeling of the process variability in ultra deep submicron SRAMs with the ultimate goal of a significantly accurate modeling of the minimum operating voltage Vmin A particular interest is also carried on the time dependent sub class of the process variability which appears as a change in the electrical characteristics of a given transistor during its operation and during its life time This research work has led to many publications and one patent application The majority of findings are retained by STMicroelectronics SRAM development team for a further use in their design optimization flow

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