Mohamed H. Abu-Rahma · Mohab Anis

Nanometer Variation-Tolerant SRAM

Circuits and Statistical Design for Yield

Springer

Nanometer Variation Tolerant Sram

Michael Brown

Nanometer Variation Tolerant Sram:

Nanometer Variation-Tolerant SRAM Mohamed Abu Rahma,Mohab Anis,2012-09-27 Variability is one of the most challenging obstacles for IC design in the nanometer regime In nanometer technologies SRAM show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density With the drastic increase in memory densities lower supply voltages and higher variations statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies Provides comprehensive review of state of the art variation tolerant SRAM circuit techniques Discusses Impact of device related process variations and how they affect circuit and system performance from a design point of view Helps designers optimize memory yield with practical statistical design methodologies and yield estimation techniques **Nanometer Variation-Tolerant Sram** ,2012-09-28 **Data Science and Applications** Satyasai Jagannath Nanda,Rajendra Prasad Yadav,Amir H. Gandomi,Mukesh Saraswat,2024-02-24 This book gathers outstanding papers presented at the International Conference on Data Science and Applications ICDSA 2023 organized by Soft Computing Research Society SCRS and Malaviya National Institute of Technology Jaipur India from 14 to 15 July 2023 The book is divided into four volumes and it covers theoretical and empirical developments in various areas of big data analytics big data technologies decision tree learning wireless communication wireless sensor networking bioinformatics and systems artificial neural networks deep learning genetic algorithms data mining fuzzy logic optimization algorithms image processing computational intelligence in civil engineering and creative computing **Microelectronics, Electromagnetics and Telecommunications** Jaume Anguera,Suresh Chandra Satapathy,Vikrant Bhateja,K.V.N. Sunitha,2018-01-25 The volume contains 94 best selected research papers presented at the Third International Conference on Micro Electronics Electromagnetics and Telecommunications ICMEET 2017 The conference was held during 09 10 September 2017 at Department of Electronics and Communication Engineering BVRIT Hyderabad College of Engineering for Women Hyderabad Telangana India The volume includes original and application based research papers on microelectronics electromagnetics telecommunications wireless communications signal speech video processing and embedded systems **Communication, Software and Networks** Vikrant Bhateja,Jnyana Ranjan Mohanty,Wendy Flores Fuentes,Koushik Maharatna,2022-10-27 This book highlights a collection of high quality peer reviewed research papers presented at the 7th International Conference on Information System Design and Intelligent Applications INDIA 2022 held at BVRIT Hyderabad College of Engineering for Women Hyderabad Telangana India from February 25 26 2022 It covers a wide range of topics in computer science and information

technology from wireless networks social networks wireless sensor networks information and network security to web security Internet of Things bioinformatics geoinformatics and computer networks VLSI Design and Test Brajesh Kumar Kaushik,Sudeb Dasgupta,Virendra Singh,2017-12-21 This book constitutes the refereed proceedings of the 21st International Symposium on VLSI Design and Test VDAT 2017 held in Roorkee India in June July 2017 The 48 full papers presented together with 27 short papers were carefully reviewed and selected from 246 submissions The papers were organized in topical sections named digital design analog mixed signal VLSI testing devices and technology VLSI architectures emerging technologies and memory system design low power design and test RF circuits architecture and CAD and design verification

Design of Variation-tolerant Circuits for Nanometer CMOS Technology Mohamed Hassan Abu-Rahma,2008 Aggressive scaling of CMOS technology in sub 90nm nodes has created huge challenges Variations due to fundamental physical limits such as random dopants fluctuation RDF and line edge roughness LER are increasing significantly with technology scaling In addition manufacturing tolerances in process technology are not scaling at the same pace as transistor s channel length due to process control limitations e g sub wavelength lithography Therefore within die process variations worsen with successive technology generations These variations have a strong impact on the maximum clock frequency and leakage power for any digital circuit and can also result in functional yield losses in variation sensitive digital circuits such as SRAM Moreover in nanometer technologies digital circuits show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density It is therefore not surprising that the International Technology Roadmap for Semiconductors ITRS lists variability as one of the most challenging obstacles for IC design in nanometer regime To facilitate variation tolerant design we study the impact of random variations on the delay variability of a logic gate and derive simple and scalable statistical models to evaluate delay variations in the presence of within die variations This work provides new design insight and highlights the importance of accounting for the effect of input slew on delay variations especially at lower supply voltages Near Threshold Computing Michael Hübner,Cristina Silvano,2015-11-14 This book explores near threshold computing NTC a design space using techniques to run digital chips processors near the lowest possible voltage Readers will be enabled with specific techniques to design chips that are extremely robust tolerating variability and resilient against errors Variability aware voltage and frequency allocation schemes will be presented that will provide performance guarantees when moving toward near threshold manycore chips Provides an introduction to near threshold computing enabling reader with a variety of tools to face the challenges of the power utilization wall Demonstrates how to design efficient voltage regulation so that each region of the chip can operate at the most efficient voltage and frequency point Investigates how performance guarantees can be ensured when moving towards NTC manycores through variability aware voltage and frequency allocation schemes **Low-Power Variation-Tolerant Design in Nanometer Silicon** Swarup

Bhunia,Saibal Mukhopadhyay,2010-11-10 Design considerations for low power operations and robustness with respect to variations typically impose contradictory requirements Low power design techniques such as voltage scaling dual threshold assignment and gate sizing can have large negative impact on parametric yield under process variations This book focuses on circuit architectural design techniques for achieving low power operation under parameter variations We consider both logic and memory design aspects and cover modeling and analysis as well as design methodology to achieve simultaneously low power and variation tolerance while minimizing design overhead This book will discuss current industrial practices and emerging challenges at future technology nodes *Nano-CMOS Circuit and Physical Design* Ban Wong,2005 Based on the authors expansive collection of notes taken over the years Nano CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing manufacturability and yield This innovative book covers process technology including sub wavelength optical lithography impact of process scaling on circuit and physical implementation and low power with leaky transistors and DFM yield and the impact of physical implementation **SRAM Leakage-power Optimization Framework** Animesh Kumar,2008 IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis ,2005 **CODES+ISSS** ,2005 **Index to IEEE Publications** Institute of Electrical and Electronics Engineers,1995 Issues for 1973 cover the entire IEEE technical literature *GLSVLSI '04* ,2004

Overcoming the Circuit Design Challenges in Nanoscale SRAMs ,2006 Most microprocessors use large on chip SRAM caches to bridge the performance gap between the processor and the main memory Due to their growing embedded applications coupled with the technology scaling challenges considerable attention is given to the design of low power and high performance SRAMs However there are many challenges in the design of both embedded and stand alone SRAMs such as the estimation and optimization of stand by power design of high speed peripheral circuits and design of robust circuits for low voltage operation Further as the technology continues scaling into the nanometer domain controlling the variation in device parameters during fabrication becomes a great challenge Variations in process parameters such as oxide thickness channel length channel width and dopant concentration can result in large variations in threshold voltage This in turn is expected to severely affect the functionality of the minimum geometry transistors that are commonly used in SRAM designs Our studies of new memory and peripheral circuits have shown significant promise in terms of power speed and robustness In this research we address the following problems 1 Circuit techniques to estimate and simultaneously reduce gate leakage and sub threshold leakage 2 Process variations tolerant design approaches to reliably sense and amplify the bitlines with a minimum discharge providing a fast and accurate readout at low power 3 Failure analysis to understand the impact of process variations soft errors leakage and noise on different memory fault mechanism to help in the design of variation tolerant low power and high performance memories 4 Design of test structures for CMOS process tuning and variation control and improvement of SRAM reliability by predicting the design yield early in the product cycle In short this

dissertation characterizes the issues in nanoscale memory design which will have a ubiquitous presence in commercial electronic market It is important for these systems to be reliable fast and consume less power thereby increasing battery life Design techniques to achieve these goals are presented *Reliability in the Face of Variability in Nanometer Embedded Memories* Shrikanth Ganapathy,2014 In this thesis we have investigated the impact of parametric variations on the behaviour of one performance critical processor structure embedded memories As variations manifest as a spread in power and performance as a first step we propose a novel modeling methodology that helps evaluate the impact of circuit level optimizations on architecture level design choices Choices made at the design stage ensure conflicting requirements from higher levels are decoupled We then complement such design time optimizations with a runtime mechanism that takes advantage of adaptive body biasing to lower power whilst improving performance in the presence of variability Our proposal uses a novel fully digital variation tracking hardware using embedded DRAM eDRAM cells to monitor run time changes in cache latency and leakage A special fine grain body bias generator uses the measurements to generate an optimal body bias that is needed to meet the required yield targets A novel variation tolerant and soft error hardened eDRAM cell is also proposed as an alternate candidate for replacing existing SRAM based designs in latency critical memory structures In the ultra low power domain where reliable operation is limited by the minimum voltage of operation Vddmin we analyse the impact of failures on cache functional margin and functional yield Towards this end we have developed a fully automated tool INFORMER capable of estimating memory wide metrics such as power performance and yield accurately and rapidly Using the developed tool we then evaluate the effectiveness of a new class of hybrid techniques in improving cache yield through failure prevention and correction Having a holistic perspective of memory wide metrics helps us arrive at design choices optimized simultaneously for multiple metrics needed for maintaining lifetime requirements **Managing and Leveraging Variations and Noise in Nanometer CMOS** Vikram B. Suresh,2015 Advanced CMOS technologies have enabled high density designs at the cost of complex fabrication process Variation in oxide thickness and Random Dopant Fluctuation RDF lead to variation in transistor threshold voltage Vth Current photo lithography process used for printing decreasing critical dimensions result in variation in transistor channel length and width A related challenge in nanometer CMOS is that of on chip random noise With decreasing threshold voltage and operating voltage and increasing operating temperature CMOS devices are more sensitive to random on chip noise in advanced technologies In this thesis we explore novel circuit techniques to manage the impact of process variation in nanometer CMOS technologies We also analyze the impact of on chip noise on CMOS circuits and propose techniques to leverage or manage impact of noise based on the application True Random Number Generator TRNG is an interesting cryptographic primitive that leverages on chip noise to generate random bits however it is highly sensitive to process variation We explore novel metastability circuits to alleviate the impact of variations and at the same time leverage on chip noise sources like Random Thermal Noise and Random Telegraph Noise

RTN to generate high quality random bits We develop stochastic models for metastability based TRNG circuits to analyze the impact of variation and noise The stochastic models are used to analyze and compare low power energy efficient and lightweight post processing techniques targeted to low power applications like System on Chip SoC and RFID We also propose variation aware circuit calibration techniques to increase reliability We extended this technique to a more generic application of designing Post Si Tunable PST clock buffers to increase parametric yield in the presence of process variation Apart from one time variation due to fabrication process transistors undergo constant change in threshold voltage due to aging wear out effects and RTN Process variation affects conventional sensors and introduces inaccuracies during measurement We present a lightweight wear out sensor that is tolerant to process variation and provides a fine grained wear out sensing A similar circuit is designed to sense fluctuation in transistor threshold voltage due to RTN Although thermal noise and RTN are leveraged in applications like TRNG they affect the stability of sensitive circuits like Static Random Access Memory SRAM We analyze the impact of on chip noise on Bit Error Rate BER and post Si test coverage of SRAM cells

Device and Circuit Techniques for Reducing Variation in Nanoscale SRAM Andrew Evert Carlson,2008

Reviewing **Nanometer Variation Tolerant Sram**: Unlocking the Spellbinding Force of Linguistics

In a fast-paced world fueled by information and interconnectivity, the spellbinding force of linguistics has acquired newfound prominence. Its capacity to evoke emotions, stimulate contemplation, and stimulate metamorphosis is really astonishing. Within the pages of "**Nanometer Variation Tolerant Sram**," an enthralling opus penned by a highly acclaimed wordsmith, readers attempt an immersive expedition to unravel the intricate significance of language and its indelible imprint on our lives. Throughout this assessment, we shall delve to the book is central motifs, appraise its distinctive narrative style, and gauge its overarching influence on the minds of its readers.

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