

# N3 ELECTRO TECHNOLOGY PAST EXAM QUESTIONS AND ANSWERS BY Mr W. KIESER

## QUESTION 1

- 1.1 Study material for Question 1 of the following parts is reproduced below (and summarised):

- 1.1.1 Question  
1.1.2 Figure  
1.1.3 Table

100  
100  
100

- 1.2 Study material for the questions of the three parts and their parts are provided, with regard to the solution of question 1 of the following 10 questions:

- 1.2.1 Question  
1.2.2 Table

100  
100

- 1.3.1 Question: (The question is reproduced in the following table, summarised and summarised for the purpose of the following 10 questions.)

- 1.3.2 Question: (The question is reproduced in the following table, summarised and summarised for the purpose of the following 10 questions.)

- 1.3.3 Question: (The question is reproduced in the following table, summarised and summarised for the purpose of the following 10 questions.)

- 1.3.4 Question: (The question is reproduced in the following table, summarised and summarised for the purpose of the following 10 questions.)

- 1.3.5 Question: (The question is reproduced in the following table, summarised and summarised for the purpose of the following 10 questions.)

## QUESTION 2

- 2.1 Study material for the following question is reproduced below (and summarised):

- 2.1.1 Question  
2.1.2 Table

100  
100

- 2.2 Study material for the following question is reproduced below (and summarised):

100

- 2.3 Study material for the following question is reproduced below (and summarised):

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100

# Leaked Papers For 2014 Electro Technology N3

**S Nieto**



### **Leaked Papers For 2014 Electro Technology N3:**

Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS Nodes Hsiao-Hsuan Liu, Francky Catthoor, 2024-12-20 Modern computing engines CPUs GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes

*Security in Computing* Charles Pfleeger, Shari Lawrence Pfleeger, Lizzie Coles-Kemp, 2023-07-24 The Art of Computer and Information Security From Apps and Networks to Cloud and Crypto Security in Computing Sixth Edition is today s essential text for anyone teaching learning and practicing cybersecurity It defines core principles underlying modern security policies processes and protection illustrates them with up to date examples and shows how to apply them in practice Modular and flexibly organized this book supports a wide array of courses strengthens professionals knowledge of foundational principles and imparts a more expansive understanding of modern security This extensively updated edition adds or expands coverage of artificial intelligence and machine learning tools app and browser security security by design securing cloud IoT and embedded systems privacy enhancing technologies protecting vulnerable individuals and groups strengthening security culture cryptocurrencies and blockchain cyberwarfare

post quantum computing and more It contains many new diagrams exercises sidebars and examples and is suitable for use with two leading frameworks the US NIST National Initiative for Cybersecurity Education NICE and the UK Cyber Security Body of Knowledge CyBOK Core security concepts Assets threats vulnerabilities controls confidentiality integrity availability attackers and attack types The security practitioner s toolbox Identification and authentication access control and cryptography Areas of practice Securing programs user internet interaction operating systems networks data databases and cloud computing Cross cutting disciplines Privacy management law and ethics Using cryptography Formal and mathematical underpinnings and applications of cryptography Emerging topics and risks AI and adaptive cybersecurity blockchains and cryptocurrencies cyberwarfare and quantum computing Register your book for convenient access to downloads updates and or corrections as they become available See inside book for details      **Alternative Press Index** ,2001      **Government Reports Announcements & Index** ,1980-11

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