```
BLCD_display_string <= (
70
   B-- ASCII hex values for LCD Display
71
    -- Enter Live Hex Data Values from hardware here
72
    -- LCD DISPLAYS THE FOLLOWING:
73
74
75
    -- UP3
76
77
    -- Line I
78
    X"41", X"30", X"0" & A(3 DOWNTO 0), X"20", X"42", X"30", X"0" & B(3 DOWNTO 0),
79
    x"20", X"53", X"3d", X"0" & S(3 DOWNTO 0), X"20", X"20", X"20", X"20", X"20",
80
     X"4F", X"75", X"74", X"70", X"75", X"74", X"30", X"0" & Hex_Display_Data(3 DOWNTO 0),
81
82
    X"20", X"20", X"20", X"20", X"20", X"20", X"20", X"20");
83
84
     -- BIDIRECTIONAL TRI STATE LCD DATA BUS
85
       DATA_BUS <= DATA_BUS_VALUE WHEN LCD_RW_INT = '0' ELSE "ZZZZZZZZZZ";
    -- get next character in display string
85
       Next_Char <= LCD_display_string(CONV_INTEGER(CHAR_COUNT));
87
88
        LCD_RW <= LCD_RW_INT;
89
   EPROCESS
90
       BEGIN
91
        WAIT UNTIL CLK_48MHZ'EVENT AND CLK_48MHZ = '1':
92 B
        IF RESET = '0' THEN
93
           CLK_COUNT_400HZ <= X"000000";
94
   CLK_400HZ_Enable <= '0':
95
   B ELSE
96
                 IF CLK_COUNT_400HZ < X"0EA60" THEN
97
                  CLK_COUNT_400HZ <= CLK_COUNT_400HZ + 1;
98
                  CLK_400HZ_Enable <= '0';
```

# **Lcd Vhdl Code De2**

Jengnan Juang, Cheng-Yi Chen, Cheng-Fu Yang

#### Lcd Vhdl Code De2:

Synthesizable VHDL Design for FPGAs Eduardo Augusto Bezerra, Djones Vinicius Lettnin, 2013-10-21 The methodology described in this book is the result of many years of research experience in the field of synthesizable VHDL design targeting FPGA based platforms VHDL was first conceived as a documentation language for ASIC designs Afterwards the language was used for the behavioral simulation of ASICs and also as a design input for synthesis tools VHDL is a rich language but just a small subset of it can be used to write synthesizable code from which a physical circuit can be obtained Usually VHDL books describe both synthesis and simulation aspects of the language but in this book the reader is conducted just through the features acceptable by synthesis tools The book introduces the subjects in a gradual and concise way providing just enough information for the reader to develop their synthesizable digital systems in VHDL The examples in the book were planned targeting an FPGA platform widely used around the world \*\*Rapid Prototyping of Digital Systems\*\* James O. Hamblen, Tyson S. Hall, Michael D. Furman, 2007-09-26 New to this edition is an introduction to embedded operating systems for SOPC designs Featuring four accelerated tutorials on the Quartus II and Nios II design environments this edition progresses from introductory programmable logic to full scale SOPC design integrating hardware implementation software development operating system support state of the art I O and IP cores This edition features Altera's new 7 1 Quartus II CAD and Nios II SOPC tools and includes projects for Altera's DE1 DE2 UP3 UP2 and UP1 FPGA development boards

Proceedings of the 2nd International Conference on Intelligent Technologies and Engineering Systems (ICITES2013)
Jengnan Juang, Cheng-Yi Chen, Cheng-Fu Yang, 2014-04-18 This book includes the original peer reviewed research papers from the conference Proceedings of the 2nd International Conference on Intelligent Technologies and Engineering Systems ICITES2013 which took place on December 12 14 2013 at Cheng Shiu University in Kaohsiung Taiwan Topics covered include laser technology wireless and mobile networking lean and agile manufacturing speech processing microwave dielectrics intelligent circuits and systems 3D graphics communications and structure dynamics and control

Technological Developments in Networking, Education and Automation Khaled Elleithy, Tarek Sobh, Magued Iskander, Vikram Kapila, Mohammad A. Karim, Ausif Mahmood, 2010-06-18 Technological Developments in Networking Education and Automation includes a set of rigorously reviewed world class manuscripts addressing and detailing state of the art research projects in the following areas Computer Networks Access Technologies Medium Access Control Network architectures and Equipment Optical Networks and Switching Telecommunication Technology and Ultra Wideband Communications Engineering Education and Online Learning including development of courses and systems for engineering technical and liberal studies programs online laboratories intelligent testing using fuzzy logic taxonomy of e courses and evaluation of online courses Pedagogy including benchmarking group learning active learning teaching of multiple subjects together ontology and knowledge management Instruction Technology including internet textbooks virtual reality labs

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of this project was to produce a VHDL design which can be programmed on the Altera DE2 board This project gives an overview of how different components of the DE2 board can be interfaced This project uses the various parts of the DE2 board like the LCD screen LEDs Push Buttons 7 segment display etc In Part 2 the main objective of the project was to produce ASIC design and optimize the design using the Synopsys tool This optimization is done using 90nm technology The target was to create design of asynchronous FIFO for n bit wide using parameter data whose default width is 16 bits Since it is asynchronous its input clock was chosen as 200 MHz and output clock as 40 MHz. This interface signals to the transmitting device when it is clear to send a burst Circuit Design and Simulation with VHDL, second edition Volnei A. Pedroni, 2010-09-17 A presentation of circuit synthesis and circuit simulation using VHDL including VHDL 2008 with an emphasis on design examples and laboratory exercises This text offers a comprehensive treatment of VHDL and its applications to the design and simulation of real industry standard circuits It focuses on the use of VHDL rather than solely on the language showing why and how certain types of circuits are inferred from the language constructs and how any of the four simulation categories can be implemented It makes a rigorous distinction between VHDL for synthesis and VHDL for simulation The VHDL codes in all design examples are complete and circuit diagrams physical synthesis in FPGAs simulation results and explanatory comments are included with the designs The text reviews fundamental concepts of digital electronics and design and includes a series of appendixes that offer tutorials on important design tools including ISE Quartus II and ModelSim as well as descriptions of programmable logic devices in which the designs are implemented the DE2 development board standard VHDL packages and other features All four VHDL editions 1987 1993 2002 and 2008 are covered This expanded second edition is the first textbook on VHDL to include a detailed analysis of circuit simulation with VHDL testbenches in all four categories nonautomated fully automated functional and timing simulations accompanied by complete practical examples Chapters 1 9 have been updated with new design examples and new details on such topics as data types and code statements Chapter 10 is entirely new and deals exclusively with simulation Chapters 11 17 are also entirely new presenting extended and advanced designs with theoretical and practical coverage of serial data communications circuits video circuits and other topics There are many more illustrations and the exercises have been updated and their number more than doubled

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