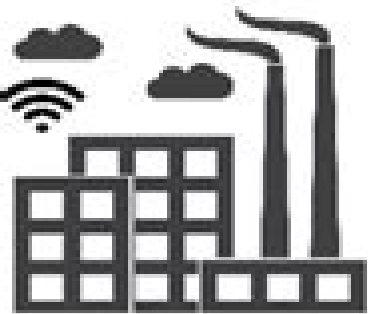




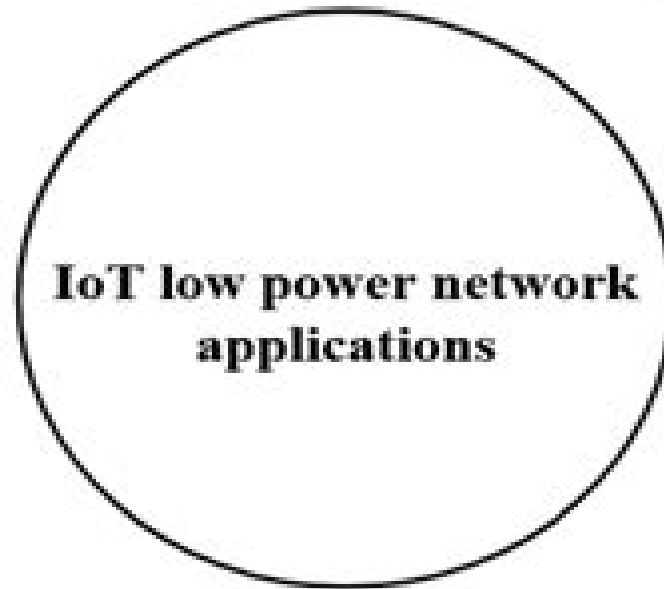
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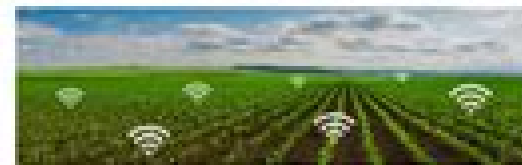
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Low Power Networks On Chip

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Networks on Chips Giovanni De Micheli, Luca Benini, 2006-08-30 The design of today s semiconductor chips for various applications such as telecommunications poses various challenges due to the complexity of these systems These highly complex systems on chips demand new approaches to connect and manage the communication between on chip processing and storage components and networks on chips NoCs provide a powerful solution This book is the first to provide a unified overview of NoC technology It includes in depth analysis of all the on chip communication challenges from physical wiring implementation up to software architecture and a complete classification of their various Network on Chip approaches and solutions Leading edge research from world renowned experts in academia and industry with state of the art technology implementations trends An integrated presentation not currently available in any other book A thorough introduction to current design methodologies and chips designed with NoCs

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contributing authors Presents an easy to comprehend writing style Optoelectronics Engineering and Information Technologies in Industry D.A. Li,W.H. Zhou,2013-09-18 Selected peer reviewed papers from the 2013 2nd International Conference on Opto Electronics Engineering and Materials Research OEMR 2013 October 19 20 2013 Zhengzhou Henan China **Machine-to-machine (M2M) Communications** Carles Anton-Haro,Mischa Dohler,2014-12-23 Part one of Machine to Machine M2M Communications covers machine to machine systems architecture and components Part two assesses performance management techniques for M2M communications Part three looks at M2M applications services and standardization Machine to machine communications refers to autonomous communication between devices or machines This book serves as a key resource in M2M which is set to grow significantly and is expected to generate a huge amount of additional data traffic and new revenue streams underpinning key areas of the economy such as the smart grid networked homes healthcare and transportation Examines the opportunities in M2M for businesses Analyses the optimisation and development of M2M communications Chapters cover aspects of access scheduling mobility and security protocols within M2M communications **High Performance and Energy Efficient Multi-core Systems for DSP Applications** Zhiyi Yu,2007 **CODES+ISSS ...** ,2006 Low Power Network-on-chip Architecture Based on Low Switching Method □□□,2007 Annales des télécommunications ,2004-07 High-Performance and Low-Power Network on Chip Switch Rabab Ezz-Eldin,Magdy A. El-Moursy,Amr M. Gody,2012 Low leakage power switch is proposed to allow saving in power dissipation of the Network on Chip NoC Two power reduction techniques are exploited to design the proposed switch The proposed NoC switch employs power supply gating to reduce the power dissipation Adaptive virtual channel AVC is proposed as a novel technique to reduce power dissipation of the NoC switch AVC technique is proposed as an efficient technique to reduce the active area using hierarchical multiplexing tree Moreover power gating reduces the average leakage power consumption of proposed switch The proposed techniques reduce the leakage and dynamic power dissipation of the switch **Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology** ,1997 3D Networks-on-Chip Architecture Optimization for Low Power Design Opoku Agyeman Michael,2015-07-13 Three dimensional Networks on Chip 3D NoCs have attracted a growing interest to solve on chip communication demands of future multi core embedded systems However 3D NoCs have not been completely accepted into the mainstream due to issues such as the high cost and complexity of manufacturing 3D vertical wires larger memory area and power consumption of 3D NoC components than that of conventional 2D NoC This thesis aims at optimizing 3D NoCs by modeling and evaluating alternate NoC topologies routing algorithms and mapping techniques to achieve optimized area power and performance parameters latency and throughput Particularly novel 3D NoC router architectures and their possible combinations have been investigated with the aim of achieving lower area and power consumption of on chip communication components with a minimal performance trade off This book investigates different heterogeneous 3D NoC architectures which combine 2D and 3D routers to improve area and

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